HIGH VOLUME, LOW COST, MMIC RECEIVER FRONT END

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ABSTRACT

Producing inexpensive MMIC receiver front ends in large quantities has focused attention on details of MMIC design and fabrication that are different from laboratory, or small volume production. This paper discusses design and testing tradeoffs and the performance of the resulting packaged MMIC.

INTRODUCTION

Pacific Monolithics has been producing a monolithic front end for 3.7-4.2 GHz satellite receivers. Extreme price pressure and large volume requirements have made this a difficult, but challenging test for the effectiveness of our new GaAs MMIC technology. With five different circuit types on the chip and 35 dB gain from RF input to IF output, cost-effectiveness has been a factor at every step in considering circuit architecture, circuit design, testing and packaging. What we have accomplished is economical production of packaged and tested GaAs MMICs. (Figure 1 shows a block diagram, and Figure 2, a photograph of the MMIC front end.)

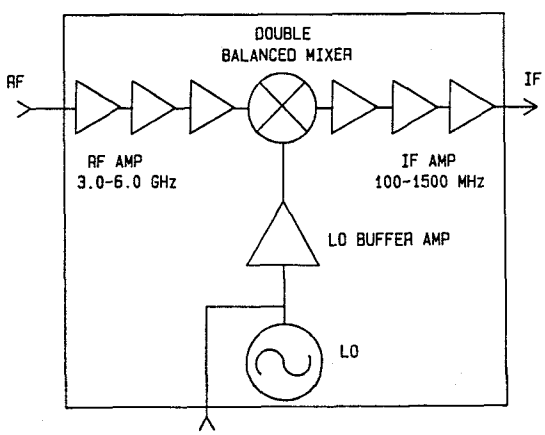

Figure 1. Block Diagram of MMIC Front End.

39 MILS

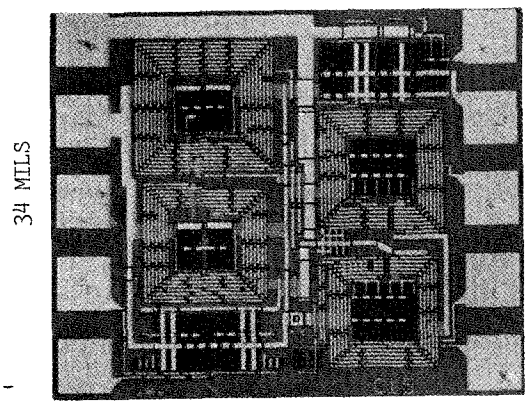

Figure 2. Photograph of MMIC Receiver Front End.

ARCHITECTURE

It was necessary to convert the 3.7-4.2 GHz band to .95-1.45 GHz in order to mate with existing receivers' capabilities. The LO frequency chosen was 5.15 GHz, rather than 2.75 GHz, to minimize the dielectric puck size and the package size. The .44" diameter puck, mounted on the "mother" board with a large (.180") spacer, stabilizes the frequency to better than ± 500 KHz over - 30 to + 60 degrees C range. Symmetrical coupling with 50 ohm microstrip lines on either side of the puck matches well with the push-pull oscillator port of the chip. Figure 3 shows the packaged chip sitting on top of the printed circuit board with the puck in its proper location, and the top cover removed.

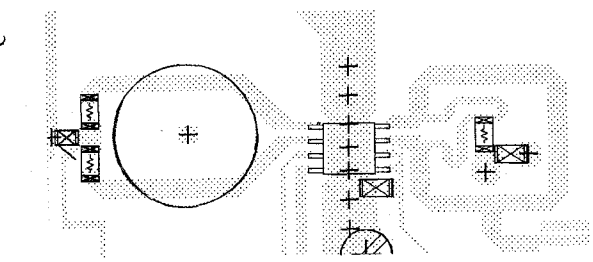

Figure 3. Packaged Chip

The RF circuits are also push-pull, helping to minimize the size of on-chip bypass capacitors, the effect of bonding and packaging inductance, and the on-chip feedback. Push-pull circuitry offers many other advantages, such as easy neutralization of capacitances, convenient coupling to balanced mixers, and broadband positive feedback for the oscillator [1,2].

Dual-gate FET mixers in the literature typically show 3 dB gain and 10 to 11 dB noise figures with 2 to 3 volt peak-to-peak LO drive voltage [3,4]. The double balanced diode mixer requires 2 volts peak-to-peak LO drive and has 7 dB conversion loss. The IF amplifier stage following has 3 dB noise figure, 10 dB gain, and a current drain of only 12 mA. The mixer/IF amplifier combination requires 2 V push-pull LO drive, has 3 dB gain and a 10 dB noise figure. A diode mixer followed by an FET IF amplifier was chosen over a dual-gate FET mixer because the combination is more tolerant of LO drive and bias and has essentially the same gain and noise figure. The diode mixer also provides a wideband resistive load which helps to stabilize the high gain RF amplifier. Figure 4 shows the input impedance of a transformer coupled RF amplifier stage with diode (resistive) and dual gate FET (capacitive) loading. A single-ended IF amplifier was used because the frequencies were lower, and the interface to the external circuitry was simpler.

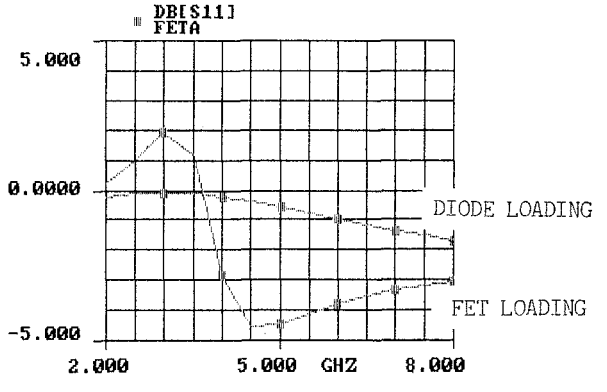

Figure 4. Input Impedance of a Transformer-Coupled RF Amplifier Stage with Diode and Dual-gate FET Loading.

CIRCUIT DESIGN

Transformer coupling was used in the RF amplifier and the LO buffer amplifier. The FETs were placed inside the transformers to get maximum space utilization [1]. At the time of conception, MIM capacitors added significantly to the cost of processing, and lowered the yield. We therefore avoided MIM capacitors and instead used N+ diodes for coupling capacitors. The push-pull RF and LO amplifiers minimized the effect of grounding inductance, allowing us to use unthinned 20 mil thick wafers and inexpensive digital packages.

Figure 5 contrasts the effect of ground lead inductance in the RF amplifier response for push-pull and single-ended designs. All the FETs were biased around 25 mA per mm, so that on-chip temperature rise was less than 20 degrees C at the hottest point in the circuit, despite the 20 mil thickness.

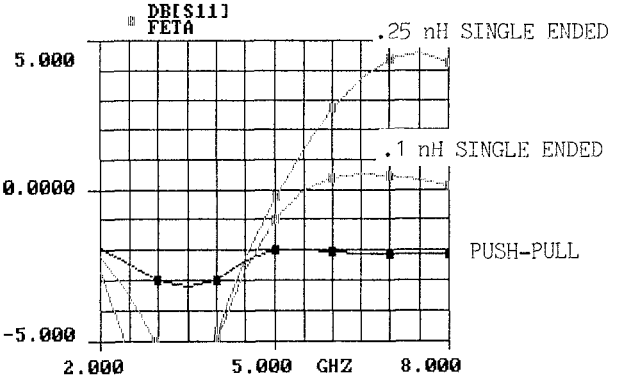

Figure 5. Effect of Ground Lead Inductance on the Return Loss of the RF Amplifier.

Clearly, we have tried to make the chip as small as possible, with coupling between inductors either minimized or utilized. Experimentally we found that coupling between adjacent spiral inductors is quite weak, as shown in Figure 6.

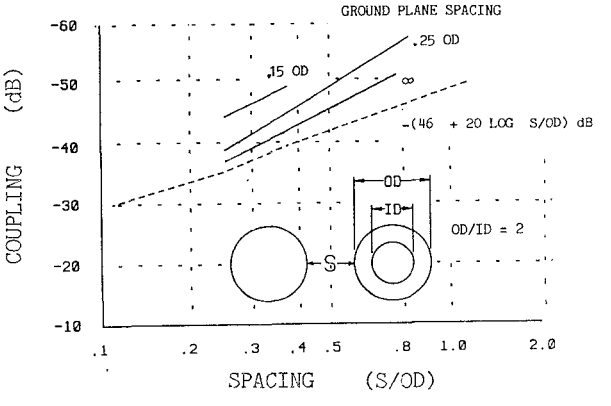

Figure 6. Coupling Between Adjacent Spiral Inductors.

TESTING

RF wafer probing at 1% level was used to establish that the wafers are RF "good". Then 100% DC wafer probing identified "good" chips for packaging. After sawing, approximately 90 % of these chips were also RF "good" when tested after they had been packaged. The production test fixtures were manually loaded; the RF, IF, and LO biases

manually set; and the 3.7-4.2 GHz gain data was captured by an IBM PC. Over 10,000 packaged parts can be tested per month by one such test station. The production test is a fully operational RF test, with FIXED TUNED RF matching network and 5.15 GHz dielectric stabilization. Figure 7 shows the measured gain of the 3-6 GHz MMIC receiver front end with a fixed 5.15 GHz LO.

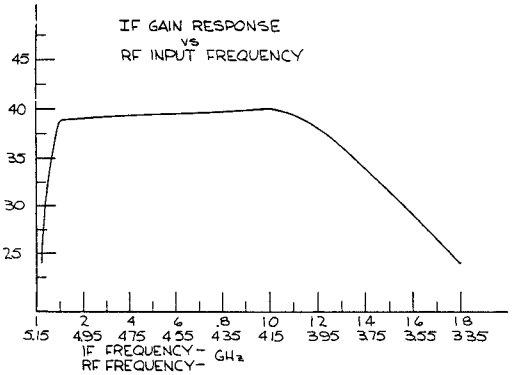

Figure 7. Measured Gain from 3-6 GHz MMIC Receiver Front End.

PACKAGING

We used small hermetic packages originally intended for digital applications. These have worked satisfactorily up to 9 GHz for our 35 dB gain receiver chips. Measurements on the package alone indicate potential problems above 10 GHz, such as seal ring resonance. Taking advantage of monolithic design, we have scaled the impedance of the circuitry on our chip to minimize the effects of the inexpensive packaging we chose, where Lp=1 nH, and Cp=.1 pF. In a recent article [5], testing and packaging are described in detail.

CONCLUSION

Low cost, high volume production of MMICs has helped us to develop process tolerant, high yield designs. Scaling these design techniques both upward and downward in frequency, we have developed .8-3 GHz and 5-8 GHz front ends with similar characteristics.

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